What is claimed is:

1. A scan test circuit comprising a noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit included in a path to be subjected to a scan test, said noninversion/inversion control circuit not inverting or inverting scan data output from said sequential circuit, on outside of said sequential circuit at arbitrary timing.

2. The scan test circuit according to claim 1, wherein said sequential circuit is a circuit that outputs the scan data as non-inverted data and inverted data, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

3. The scan test circuit according to claim 1, further comprising an inverter to generate inverted data of the scan data output from said sequential circuit, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

4. The scan test circuit according to claim 1, wherein said noninversion/inversion control circuit is a two-input exclusive OR gate circuit supplied at a first input thereof with the scan data output from said sequential circuit and supplied at a second input thereof with a noninversion/inversion control signal.

5. The scan test circuit according to claim 1, wherein said sequential circuit is a one-phase clocked sequential circuit.

6. The scan test circuit according to claim 1, wherein said sequential circuit is a two-phase clocked sequential circuit.

7. The scan test circuit according to claim 1, wherein said noninversion/inversion control circuit does not invert or inverts the scan data according to a noninversion/inversion control signal, which is input from outside.

8. The scan test circuit according to claim 7, wherein said sequential circuit is a circuit that outputs the scan data as non-inverted data and inverted data, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

9. The scan test circuit according to claim 7, further comprising an inverter to generate inverted data of the scan data output from said sequential circuit, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

10. The scan test circuit according to claim 7, wherein said noninversion/inversion control circuit is a two-input exclusive OR gate circuit supplied at a first input thereof with the scan data output from said

sequential circuit and supplied at a second input thereof with a noninversion/inversion control signal.

11. The scan test circuit according to claim 7, wherein said sequential circuit is a one-phase clocked sequential circuit.

12. The scan test circuit according to claim 8, wherein said sequential circuit is a two-phase clocked sequential circuit.

13. A scan test circuit comprising:

a first sequential circuit, with shift data corresponding to output data to be observed being set in said first sequential circuit by a scan shift conducted one repetition period before capture of the output data and scan data corresponding to the shift data being output by said first sequential circuit;

a noninversion/inversion control circuit, which does not invert or inverts the scan data output from said first sequential circuit, on outside of said first sequential circuit at arbitrary timing;

a combinational circuit included in a path to be subjected to scan test, and supplied with the scan data obtained by non-inverting or inverting the scan data by means of said noninversion/inversion control circuit; and

a second sequential circuit to capture output data output from said combinational circuit according to the scan data.

14. The scan test circuit according to claim 13, wherein said noninversion/inversion control circuit does not invert or inverts the scan data according to a noninversion/inversion control signal, which is input from outside.

15. The scan test circuit according to claim 13, wherein said first sequential circuit is a circuit that outputs the scan data as non-inverted data and inverted data, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

16. The scan test circuit according to claim 13, further comprising an inverter to generate inverted data of the scan data output from said first sequential circuit, said noninversion/inversion control circuit being a multiplexer that outputs selectively the non-inverted data or inverted data of the scan data according to a noninversion/inversion control signal, which is input from outside.

17. The scan test circuit according to claim 13, wherein said noninversion/inversion control circuit is a two-input exclusive OR gate circuit supplied at a first input thereof with the scan data output from said first sequential circuit and supplied at a second input thereof with a noninversion/inversion control signal.

18. The scan test circuit according to claim 13, wherein CTS (Clock Tree Synthesis) processing is conducted so as to cause state transition simultaneously in a clock supply external terminal used to supply a clock to each of said sequential circuits and a clock input of the corresponding sequential circuit, and CTS processing is conducted so as to cause state transition simultaneously in a control signal supply external terminal used to supply the noninversion/inversion control signal to said noninversion/inversion control

circuit and a noninversion/inversion control signal input of said noninversion/inversion control circuit.

19. The scan test circuit according to claim 13, wherein said first and second sequential circuits are one-phase clocked sequential circuits.

20. The scan test circuit according to claim 13, wherein said first and second sequential circuits are two-phase clocked sequential circuits.